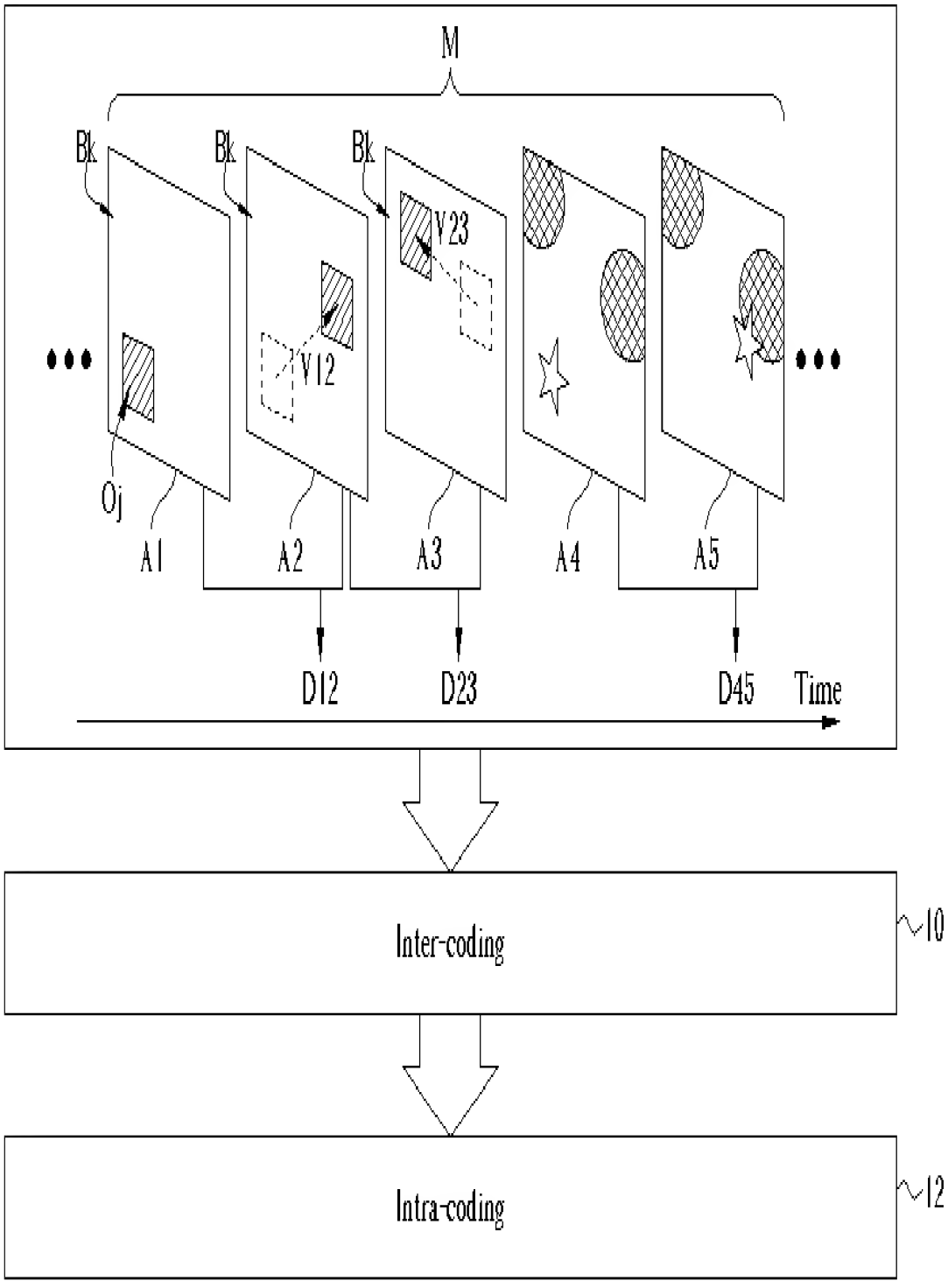
M
Bk
Bk
Bk
V23
V12
Oj
A1
A2
A3
A4
A5
D12
D23
D45
Time
Inter-coding
10
Intra-coding
12

Fig. 1

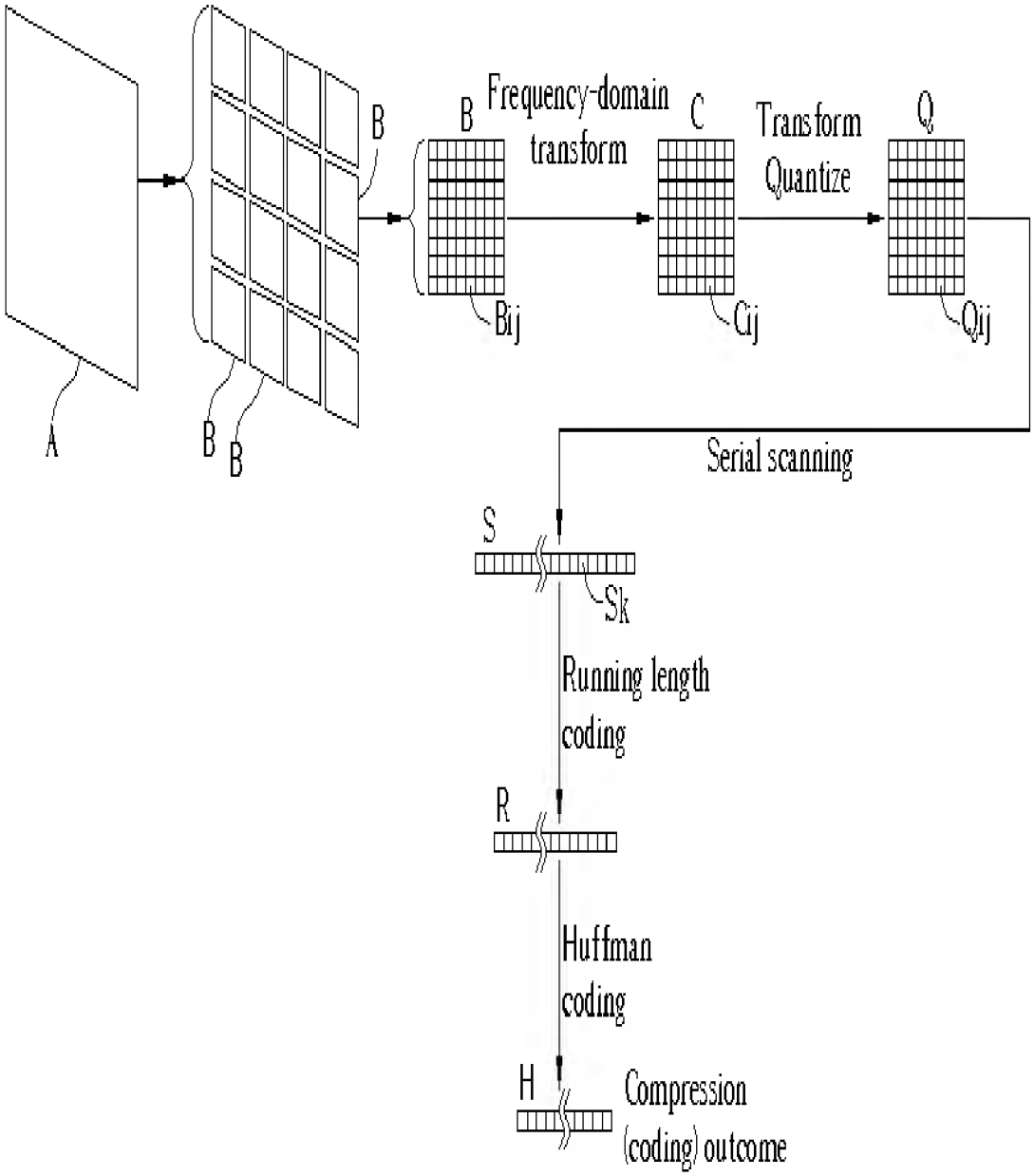
A
B
B
B
B
Frequency-domain
transform
C
Transform
Quantize
Q
Bij
Cij
Qij
Serial scanning
S
Sk
Running length
coding
R
Huffman
coding
H
Compression
(coding) outcome

Fig. 2

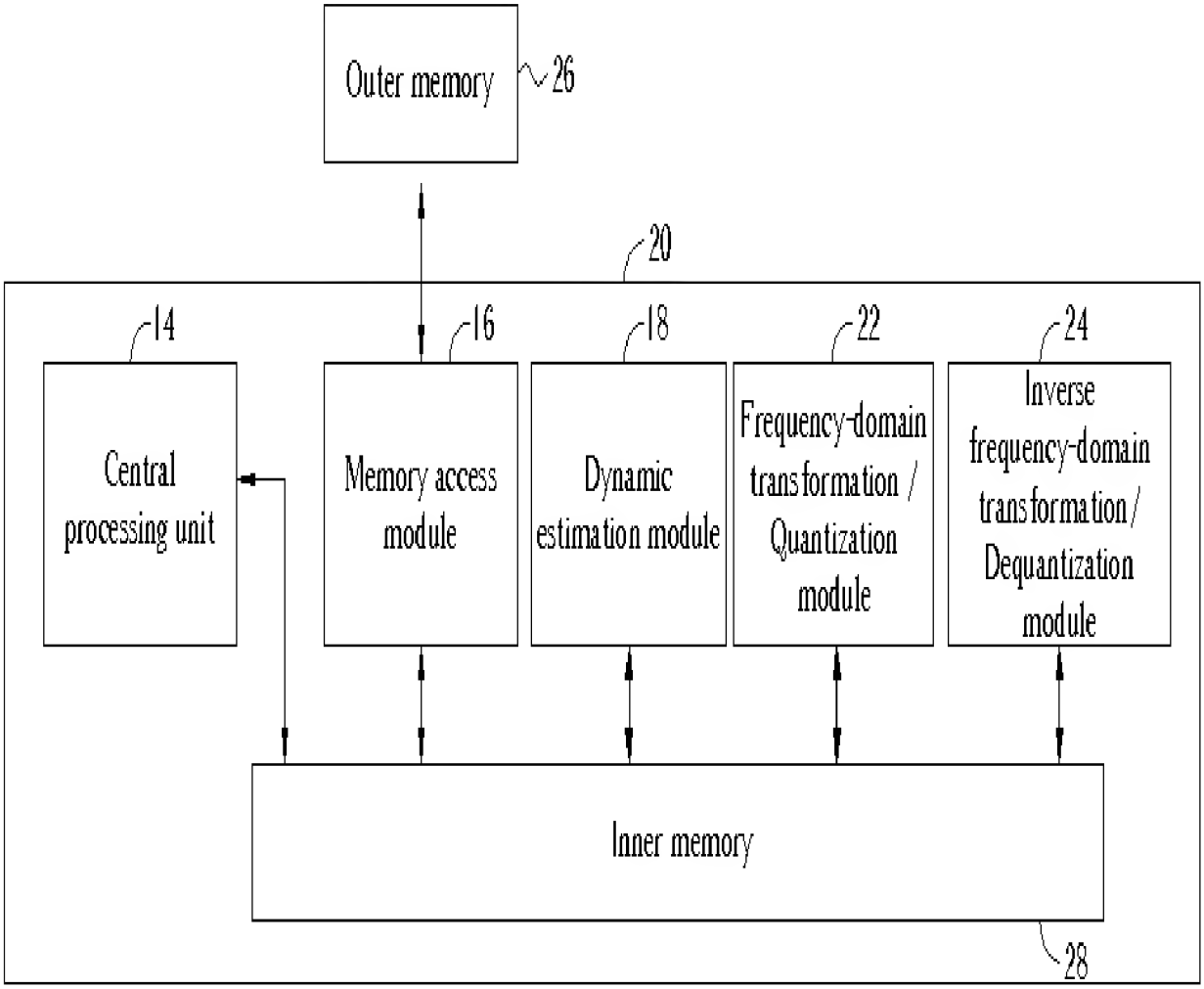
Outer memory
26
20
14
16
18
22
24
Central processing unit
Memory access module
Dynamic estimation module
Frequency-domain transformation / Quantization module
Inverse frequency-domain transformation / Dequantization module
Inner memory
28

Fig. 3

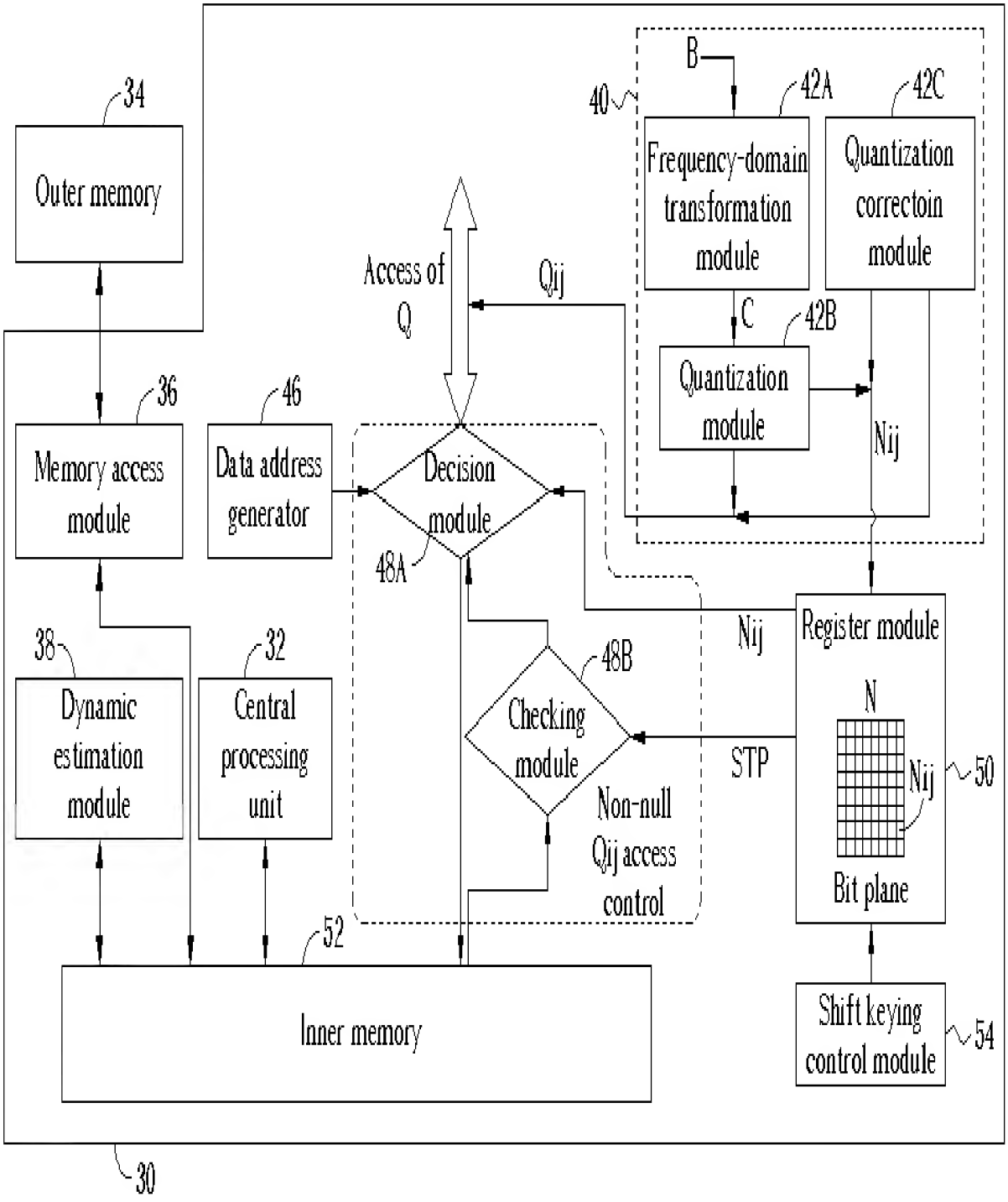
34
Outer memory
36
Memory access module
46
Data address generator
38
Dynamic estimation module
32
Central processing unit
52
Inner memory
30
Access of Q
Qij
Decision module
48A
40
B
42A
Frequency-domain transformation module
42C
Quantization correctoin module
C
42B
Quantization module
Nij
Nij
Register module
N
Nij
50
Bit plane
48B
Checking module
STP
Non-null Qij access control
Shift keying control module
54

Fig. 4

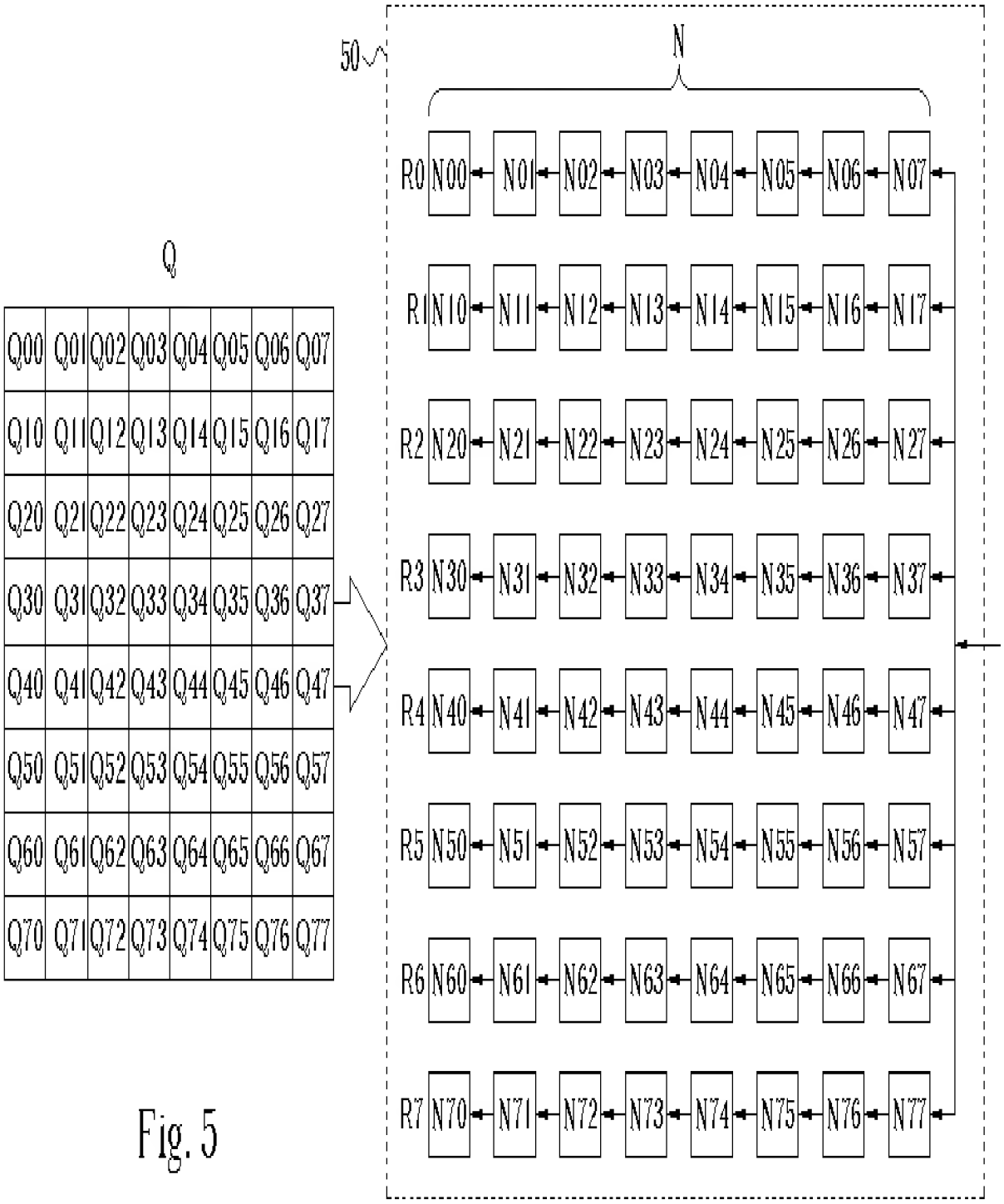
50
N
Q
R0 N00 N01 N02 N03 N04 N05 N06 N07
R1 N10 N11 N12 N13 N14 N15 N16 N17
R2 N20 N21 N22 N23 N24 N25 N26 N27
R3 N30 N31 N32 N33 N34 N35 N36 N37
R4 N40 N41 N42 N43 N44 N45 N46 N47
R5 N50 N51 N52 N53 N54 N55 N56 N57
R6 N60 N61 N62 N63 N64 N65 N66 N67
R7 N70 N71 N72 N73 N74 N75 N76 N77
Q00 Q01 Q02 Q03 Q04 Q05 Q06 Q07
Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17
Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27
Q30 Q31 Q32 Q33 Q34 Q35 Q36 Q37
Q40 Q41 Q42 Q43 Q44 Q45 Q46 Q47
Q50 Q51 Q52 Q53 Q54 Q55 Q56 Q57
Q60 Q61 Q62 Q63 Q64 Q65 Q66 Q67
Q70 Q71 Q72 Q73 Q74 Q75 Q76 Q77

Fig. 5

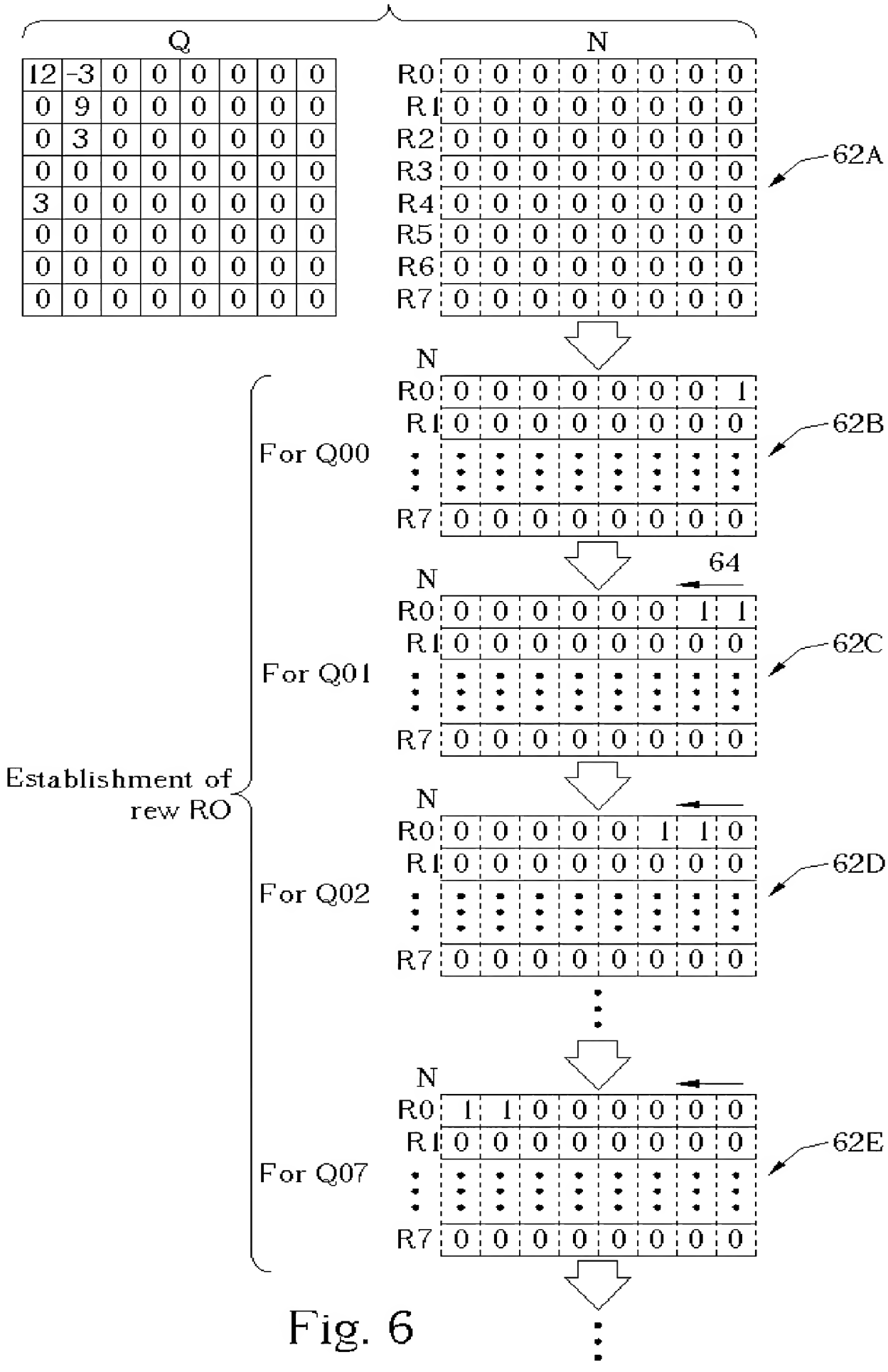
Q
N
12 -3 0 0 0 0 0 0
0 9 0 0 0 0 0 0
0 3 0 0 0 0 0 0
0 0 0 0 0 0 0 0
3 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
R0 0 0 0 0 0 0 0 0
R1 0 0 0 0 0 0 0 0
R2 0 0 0 0 0 0 0 0
R3 0 0 0 0 0 0 0 0
R4 0 0 0 0 0 0 0 0
R5 0 0 0 0 0 0 0 0
R6 0 0 0 0 0 0 0 0
R7 0 0 0 0 0 0 0 0
62A
Establishment of rew RO
For Q00
For Q01
For Q02
For Q07
N
R0 0 0 0 0 0 0 0 1
R1 0 0 0 0 0 0 0 0
R7 0 0 0 0 0 0 0 0
62B
64
R0 0 0 0 0 0 0 1 1
62C
R0 0 0 0 0 0 1 1 0
62D
R0 1 1 0 0 0 0 0 0
62E

Fig. 6

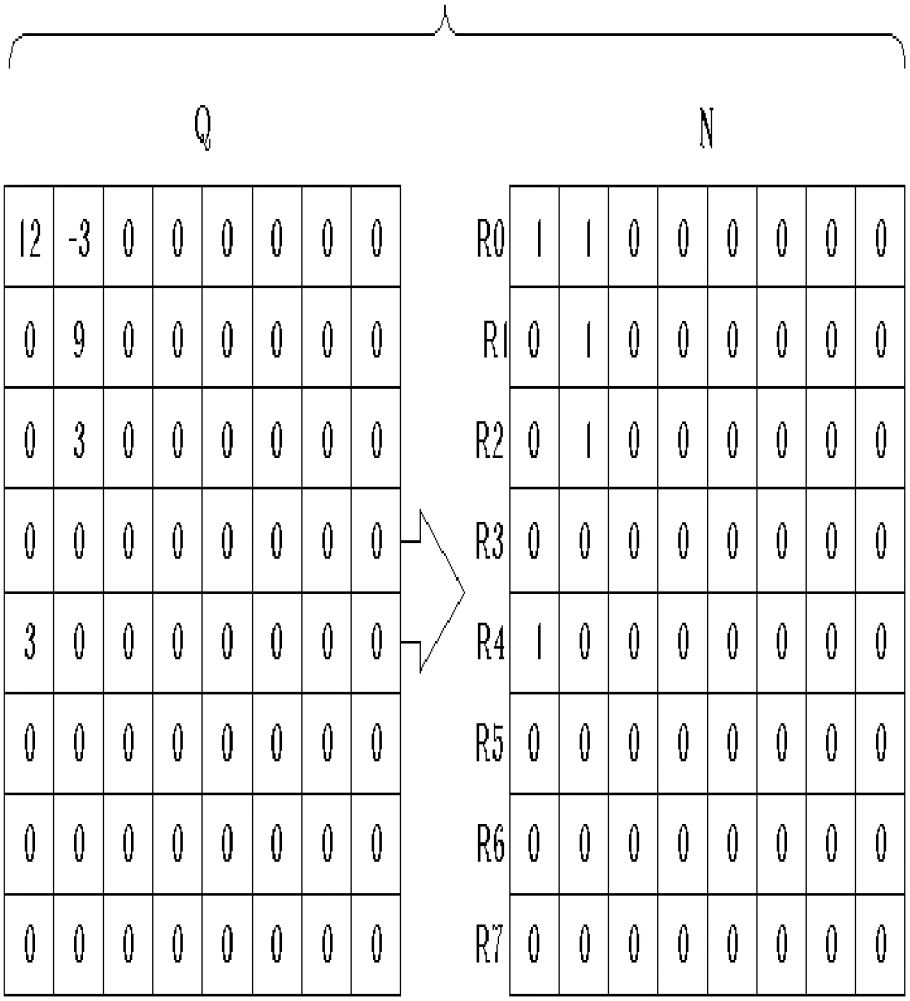
Q
N
12 -3 0 0 0 0 0 0
0 9 0 0 0 0 0 0
0 3 0 0 0 0 0 0
0 0 0 0 0 0 0 0
3 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
R0 1 1 0 0 0 0 0 0
R1 0 1 0 0 0 0 0 0
R2 0 1 0 0 0 0 0 0
R3 0 0 0 0 0 0 0 0
R4 1 0 0 0 0 0 0 0
R5 0 0 0 0 0 0 0 0
R6 0 0 0 0 0 0 0 0
R7 0 0 0 0 0 0 0 0

Fig. 7

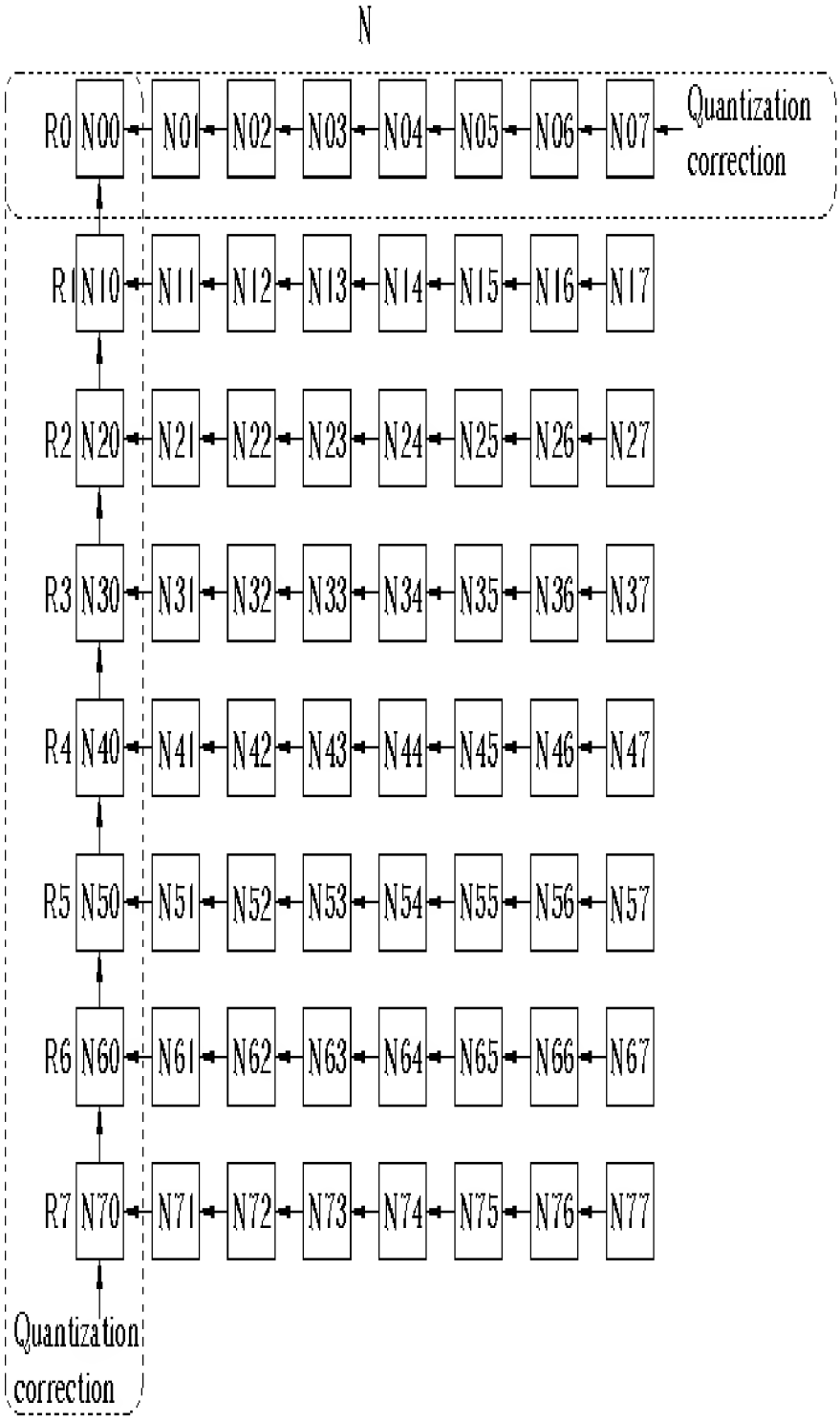
N
R0
N00
N01
N02
N03
N04
N05
N06
N07
Quantization correction
R1
N10
N11
N12
N13
N14
N15
N16
N17
R2
N20
N21
N22
N23
N24
N25
N26
N27
R3
N30
N31
N32
N33
N34
N35
N36
N37
R4
N40
N41
N42
N43
N44
N45
N46
N47
R5
N50
N51
N52
N53
N54
N55
N56
N57
R6
N60
N61
N62
N63
N64
N65
N66
N67
R7
N70
N71
N72
N73
N74
N75
N76
N77
Quantization correction

Fig. 8

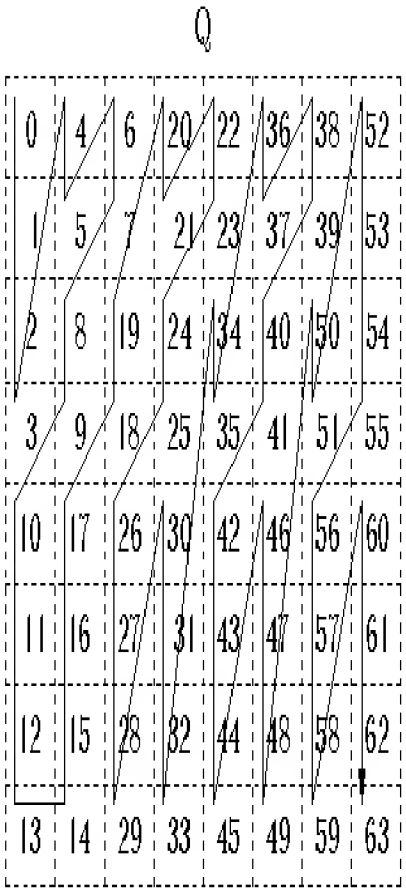
Q
0 4 6 20 22 36 38 52
1 5 7 21 23 37 39 53
2 8 19 24 34 40 50 54
3 9 18 25 35 41 51 55
10 17 26 30 42 46 56 60
11 16 27 31 43 47 57 61
12 15 28 32 44 48 58 62
13 14 29 33 45 49 59 63

Fig. 9

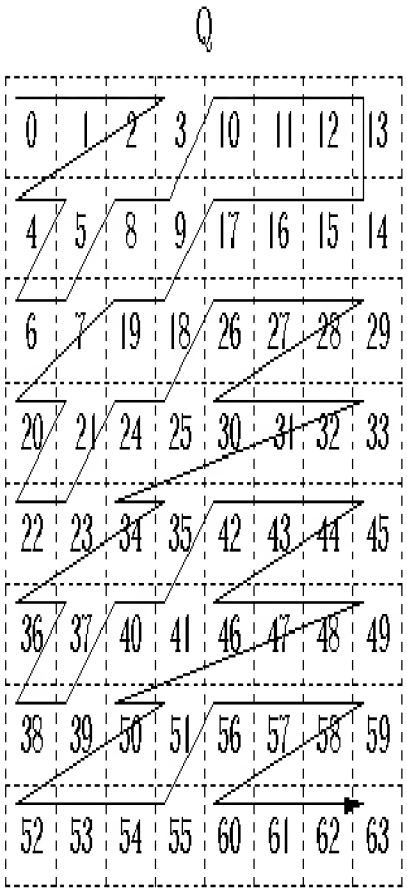
Q
0 1 2 3 10 11 12 13
4 5 8 9 17 16 15 14
6 7 19 18 26 27 28 29
20 21 24 25 30 31 32 33
22 23 34 35 42 43 44 45
36 37 40 41 46 47 48 49
38 39 50 51 56 57 58 59
52 53 54 55 60 61 62 63

Fig. 10

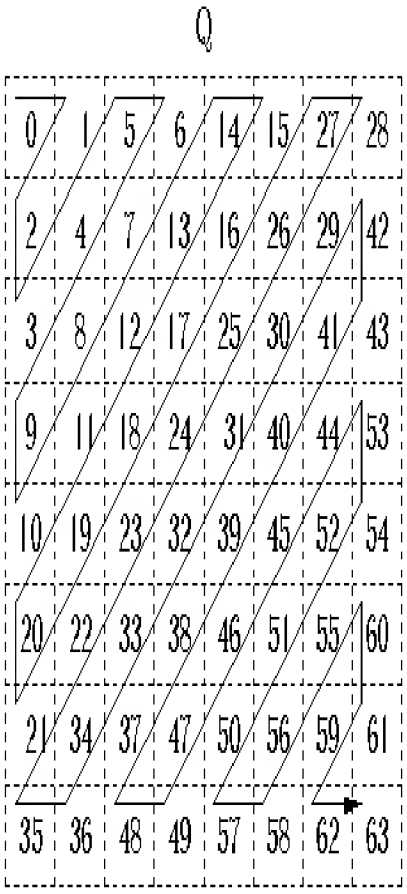
Q
0 1 5 6 14 15 27 28
2 4 7 13 16 26 29 42
3 8 12 17 25 30 41 43
9 11 18 24 31 40 44 53
10 19 23 32 39 45 52 54
20 22 33 38 46 51 55 60
21 34 37 47 50 56 59 61
35 36 48 49 57 58 62 63

Fig. 11

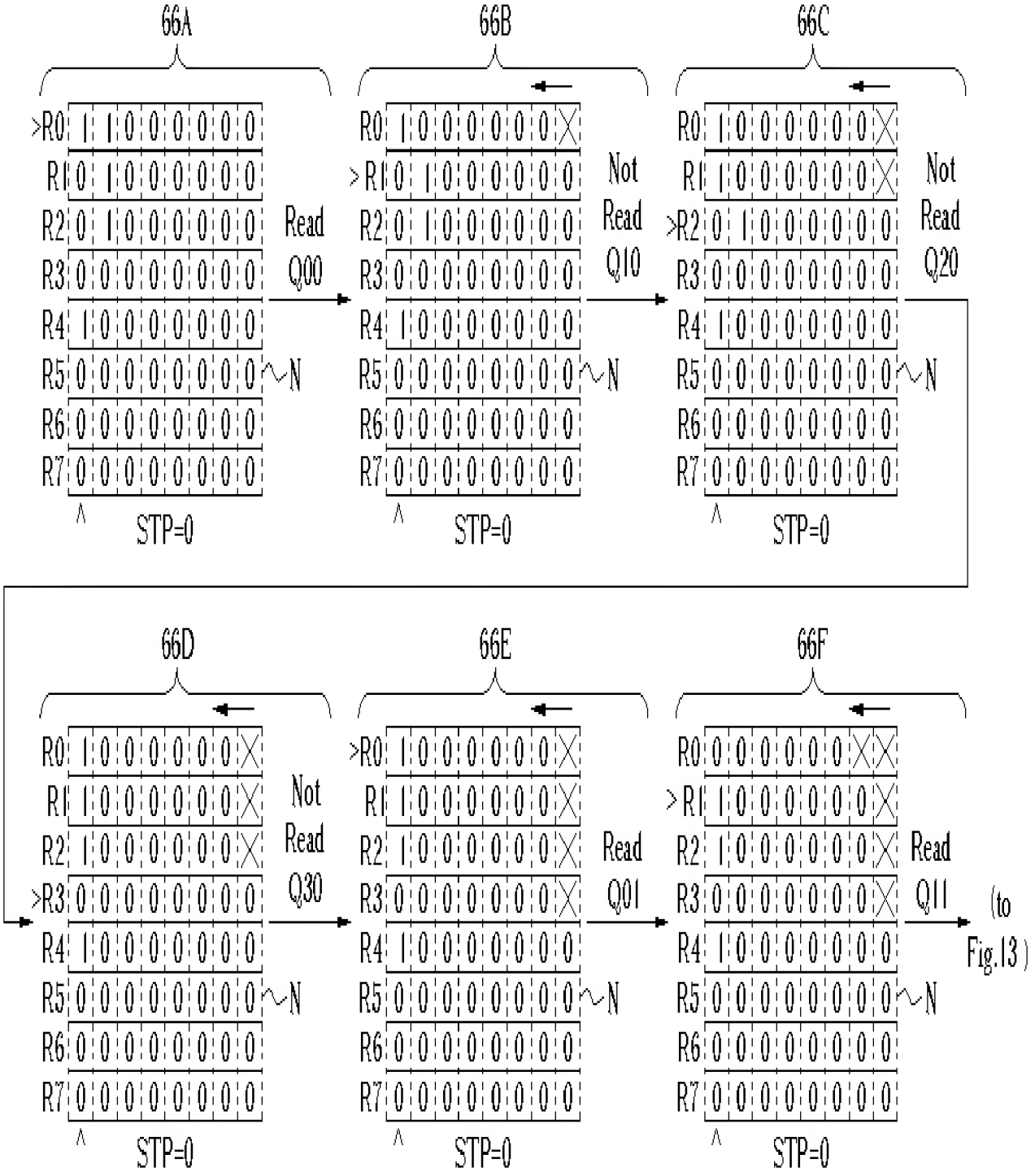
66A
66B
66C
66D
66E
66F
R0
R1
R2
R3
R4
R5
R6
R7
STP=0
N
Read
Q00
Not
Read
Q10
Not
Read
Q20
Not
Read
Q30
Read
Q01
Read
Q11
(to
Fig.13)

Fig. 12

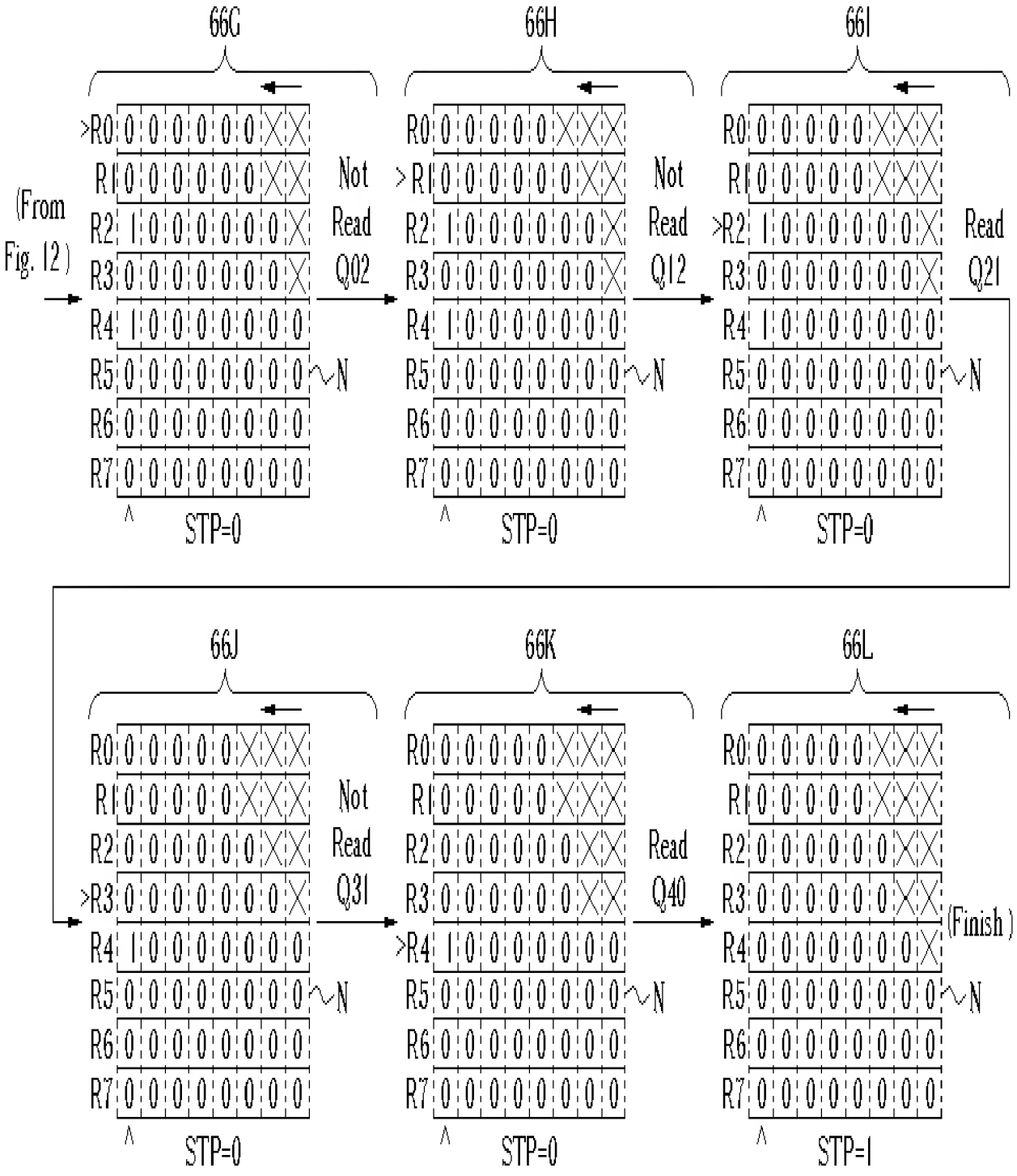
66G
66H
66I
66J
66K
66L
(From Fig. 12)
Not Read Q02
Not Read Q12
Read Q21
Not Read Q31
Read Q40
(Finish)
STP=0
STP=1
N

Fig. 13

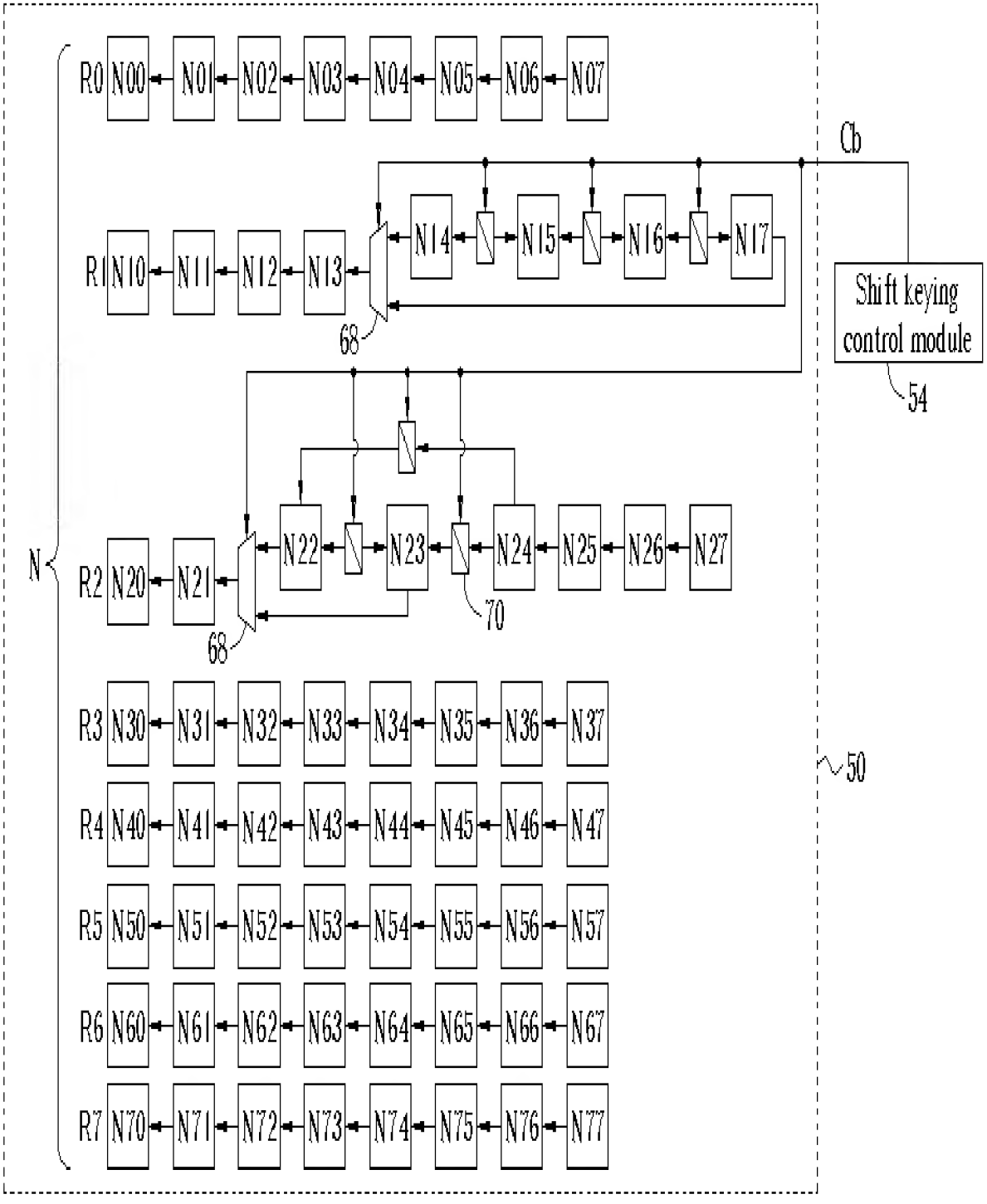
R0 N00 N01 N02 N03 N04 N05 N06 N07
R1 N10 N11 N12 N13 N14 N15 N16 N17
68
Cb
Shift keying control module
54
N
R2 N20 N21 N22 N23 N24 N25 N26 N27
70
68
R3 N30 N31 N32 N33 N34 N35 N36 N37
R4 N40 N41 N42 N43 N44 N45 N46 N47
R5 N50 N51 N52 N53 N54 N55 N56 N57
R6 N60 N61 N62 N63 N64 N65 N66 N67
R7 N70 N71 N72 N73 N74 N75 N76 N77
50

Fig. 14

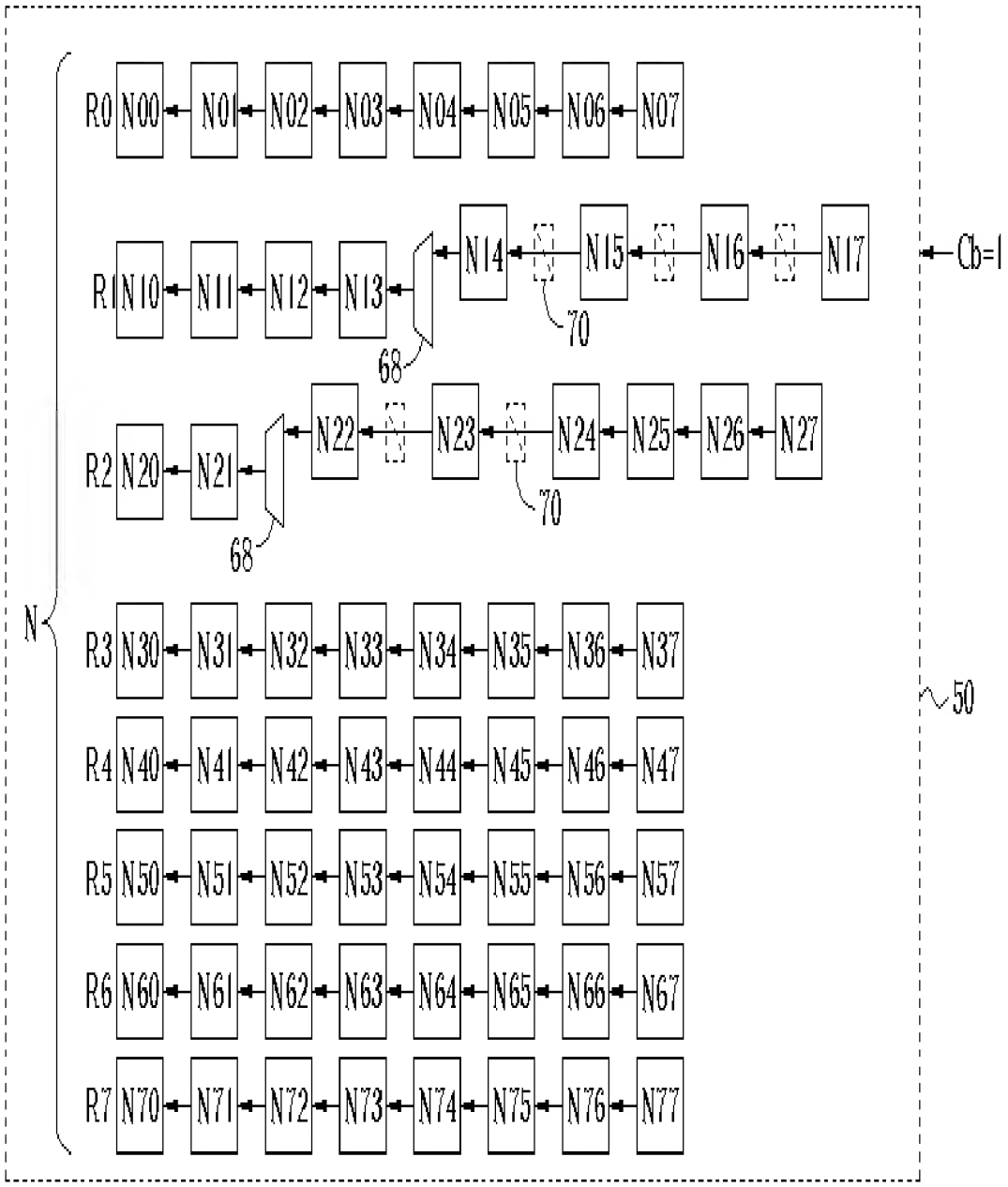
R0
N00
N01
N02
N03
N04
N05
N06
N07
R1
N10
N11
N12
N13
N14
N15
N16
N17
Cb=1
70
68
R2
N20
N21
N22
N23
N24
N25
N26
N27
70
68
N
R3
N30
N31
N32
N33
N34
N35
N36
N37
R4
N40
N41
N42
N43
N44
N45
N46
N47
R5
N50
N51
N52
N53
N54
N55
N56
N57
R6
N60
N61
N62
N63
N64
N65
N66
N67
R7
N70
N71
N72
N73
N74
N75
N76
N77
50

Fig. 15

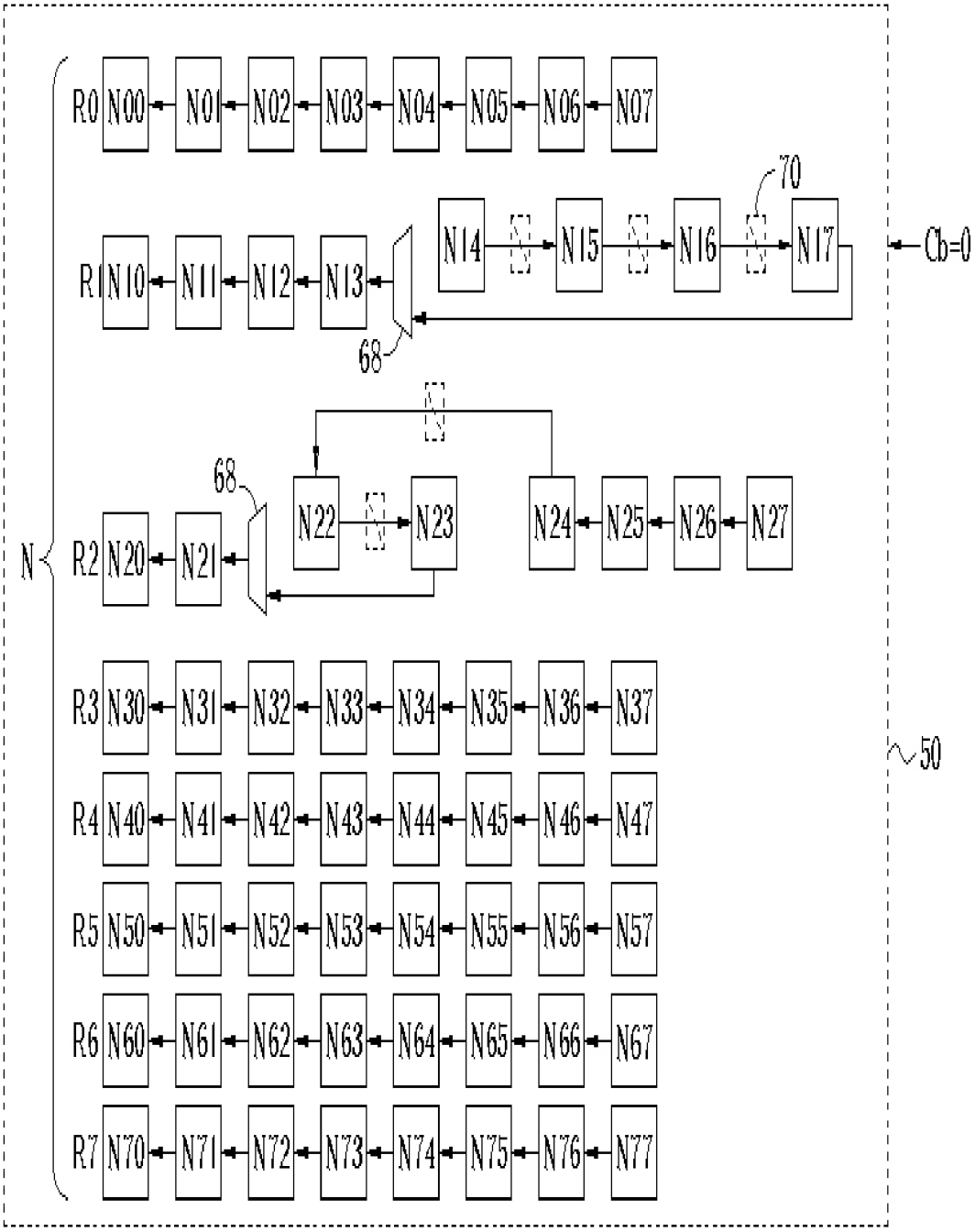
N
R0
N00
N01
N02
N03
N04
N05
N06
N07
R1
N10
N11
N12
N13
N14
N15
N16
N17
70
Cb=0
68
R2
N20
N21
N22
N23
N24
N25
N26
N27
R3
N30
N31
N32
N33
N34
N35
N36
N37
R4
N40
N41
N42
N43
N44
N45
N46
N47
R5
N50
N51
N52
N53
N54
N55
N56
N57
R6
N60
N61
N62
N63
N64
N65
N66
N67
R7
N70
N71
N72
N73
N74
N75
N76
N77
50

Fig. 16

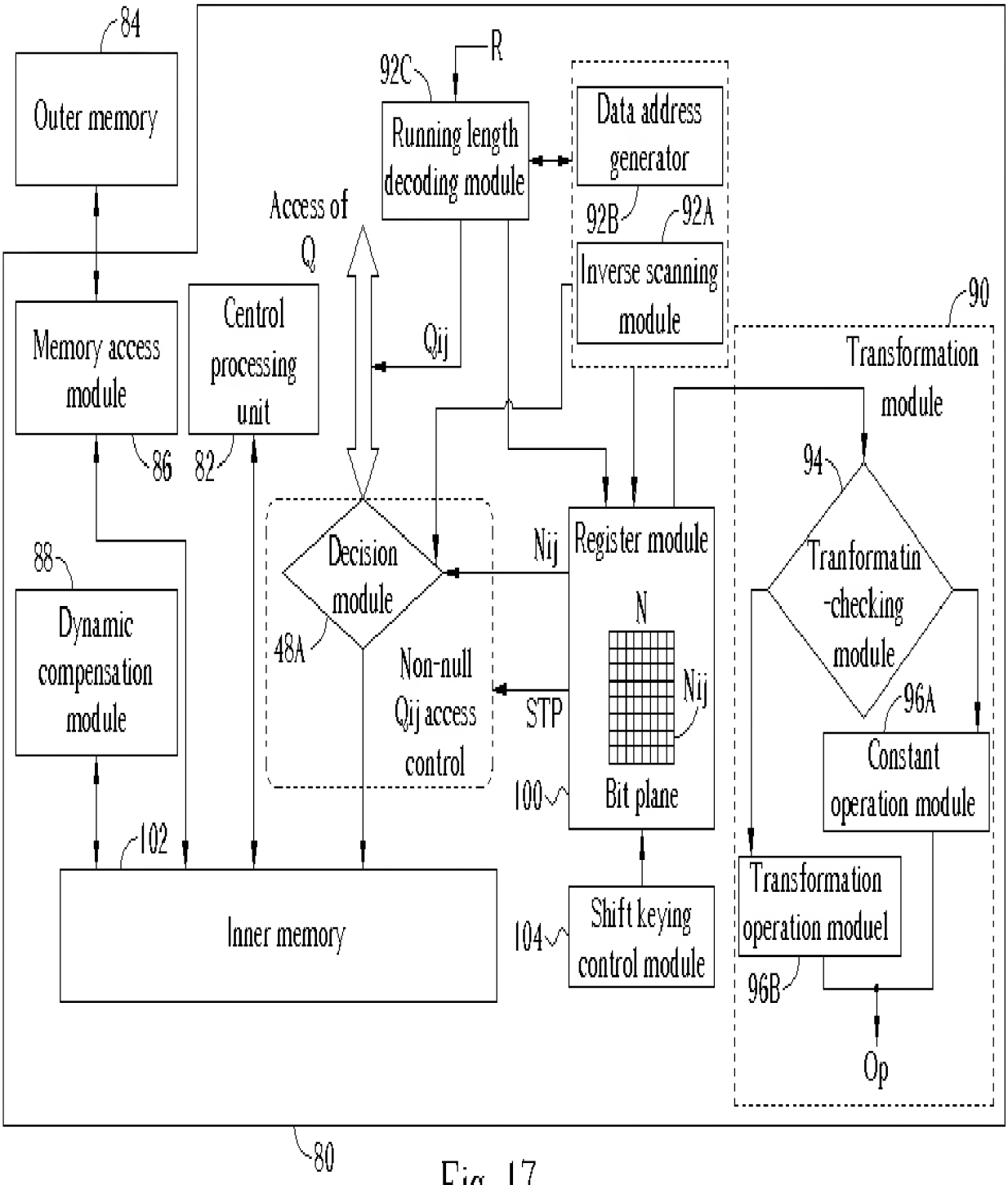
84
Outer memory
92C
R
Running length decoding module
Data address generator
92B
92A
Inverse scanning module
Access of Q
Qij
Centrol processing unit
Memory access module
86
82
90
Transformation module
94
Tranformatin -checking module
96A
Constant operation module
Transformation operation moduel
96B
Op
Decision module
48A
Nij
Register module
N
Nij
Bit plane
100
STP
Non-null Qij access control
88
Dynamic compensation module
102
Inner memory
104
Shift keying control module
80

Fig. 17

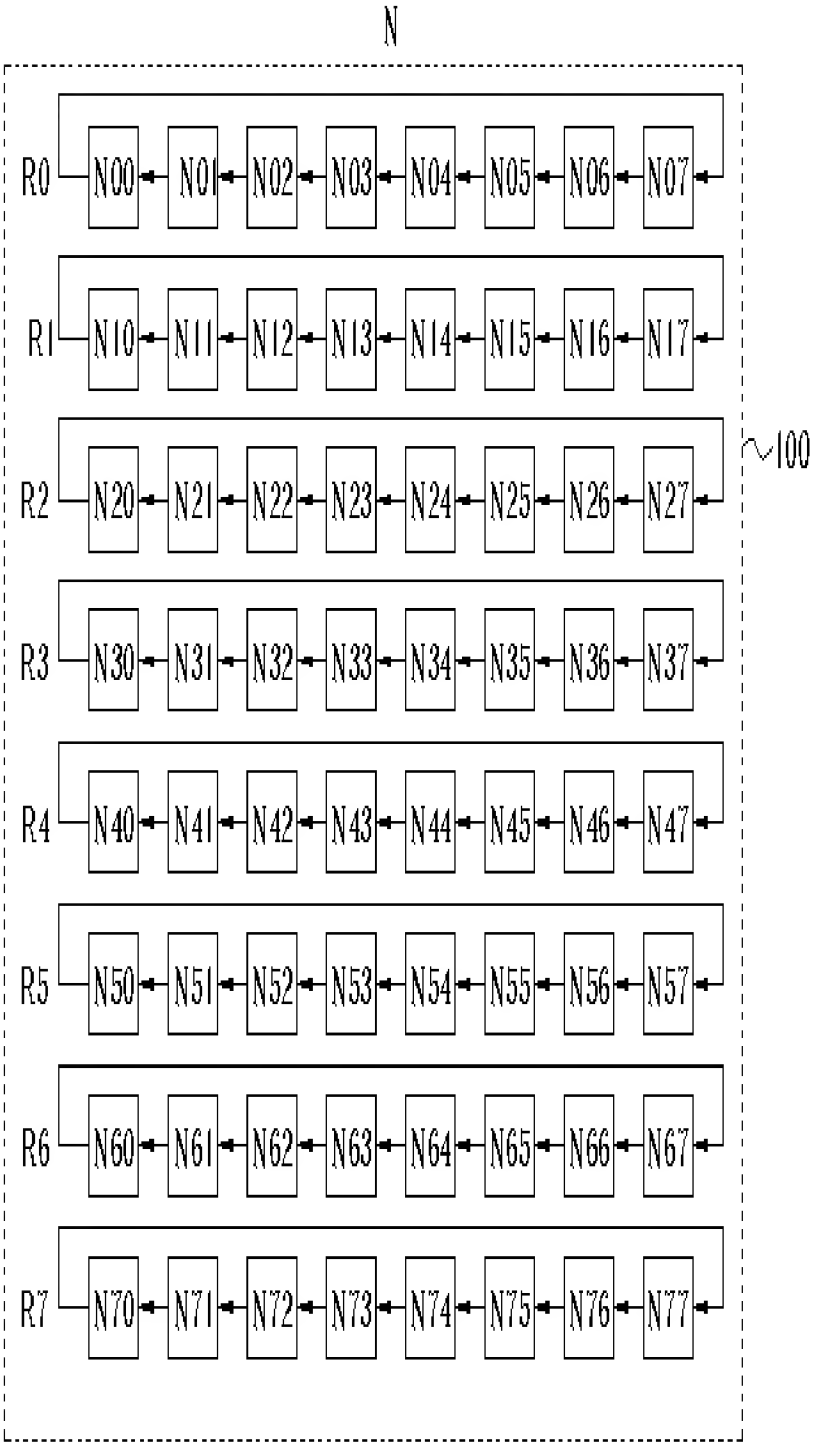
N
R0
N00
N01
N02
N03
N04
N05
N06
N07
R1
N10
N11
N12
N13
N14
N15
N16
N17
R2
N20
N21
N22
N23
N24
N25
N26
N27
100
R3
N30
N31
N32
N33
N34
N35
N36
N37
R4
N40
N41
N42
N43
N44
N45
N46
N47
R5
N50
N51
N52
N53
N54
N55
N56
N57
R6
N60
N61
N62
N63
N64
N65
N66
N67
R7
N70
N71
N72
N73
N74
N75
N76
N77

Fig. 18

```
/* bit  Nm0, Nm1, ... Nm7  corresponding to frequency domain data element Bm0, Bm1, ... Bm7 */


if ( Nm1|Nm2|Nm3|Nm4|Nm5|Nm6|Nm7=0 )
{  Op0=Op1=Op2=Op3=Op4=Op5=Op6=Op7=C0 }
else
{  Calculate Op by inverse One-dimensional frequency-domain transformation  }
```

Fig. 19